TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7USB221FT

Dual SPDT USB Switch

TC7USB221 is high-speed CMOS dual 1-2 multiplexer /demultiplexer. The low on resistance and the low capacitance of the switch allow connections to USB application.

This device consists of dual individual two-inputs multiplexer/demultiplexer with common select input (S) and output enable (\overline{OE}). The D+/D- inputs is connected to the D1+/D1- or D2+/D2- outputs determined by the combination both the select input (S) and output enable (\overline{OE}). When the output enable (\overline{OE}) input is held "H" level, the switches are open with regardless the state of select inputs and a high-impedance state exists between the switches.

All inputs are equipped with protection circuits against static discharge.

Features

- Operating voltage: V_{CC} = 2.3 to 3.6 V
- ON-capacitance: $C_{I/O} = 7 \text{ pF}$ Switch ON (typ.) @V_{CC}=3.3 V
- ON-resistance: $R_{ON} = 6.5 \Omega$ (typ.) @ V_{CC}=3 V, V_{I/O}=0 V
- Ron Flatness: $R_{ON(flat)} = 1.6 \Omega$ (typ.) @ V_{CC}=3 V
- Delta Ron: $\Delta R_{ON} = 0.5 \Omega$ (typ.) @ V_{CC}=3 V
- ESD performance: Machine model $\geq \pm 200 \text{ V}$

Human body model $\geq \pm 2000 \text{ V}$

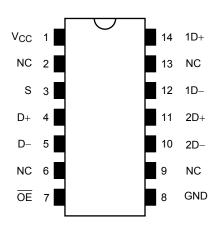
- Power-down protection for inputs (OE and S, I/O)
- Package: TSSOP14

TC7USB221FT TSSOP14-P-0044-0.65A Weight

TSSOP14-P-0044-0.65A: 0.06 g (typ.)

Pin Assignment (top view)

FT (TSSOP14-P-0044-0.65A)

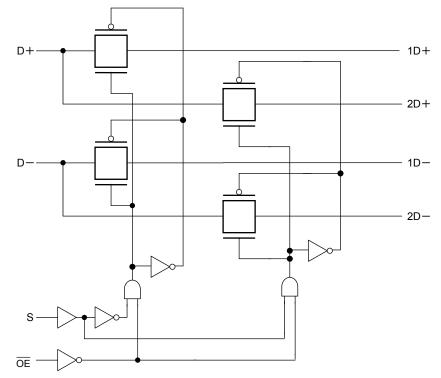


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Truth Table

Inputs		Function				
ŌĒ	S					
L	L	D+ port = 1D+ port, D- Port = 1D- Port				
L	Н	D+ port = 2D+ port, D- Port = 2D- Port				
Н	Х	Disconnect				

System Diagram



Absolute Maximum Ratings (Note)

Characte	eristic	Symbol	Rating	Unit
Power supply range		V _{CC}	-0.5 to 4.6	V
Control pin input voltage	(OE , S)	VIN	-0.5 to 4.6	V
Switch terminal I/O voltage	V _{CC} =0 V or Switch=Off	M	-0.5 to 4.6	V
	Switch=On	VS	–0.5 to V _{CC} +0.5	v
Clump diode current	Control input	lu e	-50	mA
	Switch	IК	±50	ША
Switch I/O current		IS	50	mA
Power dissipation		PD	PD 180	
DC V _{CC} /GND current		I _{CC} /I _{GND}	±100	mA
Storage temperature		T _{stg}	–65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction. Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Charact	eristic	Symbol	Rating	Unit
Power supply voltage		V _{CC}	2.3 to 3.6	V
Control pin input voltage	(OE , S)	VIN	0 to 3.6	V
Switch I/O weltere	V _{CC} =0 V or Switch=Off		0 to 3.6	V
Switch I/O voltage	Switch=On	VS	0 to V _{CC}	v
Operating temperature		T _{opr}	-40 to 85	°C
Input rise and fall time		dt/dv	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C)

Characteristics		Symbol	Test Condition V _{CC} (V)		Min	Тур.	Max	Unit
Input voltage	"H" level	VIH	—	2.3 to 3.6	$0.46 \times V_{CC}$	_	_	V
(OE , S)	"L" level	V _{IL}	_	2.3 to 3.6	_	_	0.25 × V _{CC}	v
Input leakage current (OE , S)		I _{IN}	$V_{IN} = 0$ to 3.6 V	2.3 to 3.6		_	±1.0	μA
Power-off leakage current		I _{OFF}	V _{IN} = 0 to 3.6 V	0	_	_	±5.0	μA
Off-state leakage current (switch off)		I _{SZ}	D+, D- = 0 to V _{CC} , $\overline{OE} = V_{CC}$	2.3 to 3.6	_	_	±5.0	μA
			$V_{IS} = 0 \text{ V}, \text{ I}_{IS} = 30 \text{ mA} \qquad (\text{Note1})$	3.0		6.5	10	
ON resistance	(Note2)	R _{ON}	$V_{IS} = 0.4 \text{ V}, I_{IS} = 30 \text{ mA}$ (Note1)	3.0		7.0	11	Ω
(Notez)			$V_{IS} = 3.0 \text{ V}, I_{IS} = 30 \text{ mA}$ (Note1)	3.0	_	13	19	I
Delta R _{ON}		ΔR_{ON}	$V_{IS} = 0.4 V$, 1.0 V, $I_{IS} = 30 mA$ 3.0		_	0.5	_	Ω
On-Resistance Flatness		R _{ON(flat)}	V_{IN} = 0 V to 1.0 V, I_{IS} = 30 mA 3.0		_	1.6	_	Ω
Quiescent supply current		ICC	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$ 3.6		_		2.0	μA
Increase in I _{CC} per input		ΔI_{CC}	V _{IN} = 1.8 V	3.6			10.0	μA

Note1: All typical values are at $Ta = 25^{\circ}C$.

Note2: Measured by the voltage drop between D+/D- and 1D+/1D-, 2D+/2D- pins at the indicated current through the switch. ON resistance is determined by the lower of the voltages on the two pins.

AC Characteristics V_{CC} =3.3V±10% (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Тур.	Max	Unit
Propagation Delay Time (Note)	tpd	C _L =5 pF	$\textbf{3.3}\pm\textbf{0.3}$	_	0.25	_	ns
Turn ON Time (S, \overline{OE} to Output)	t _{ON}	R _L =50 Ω, C _L =5 pF	$\textbf{3.3}\pm\textbf{0.3}$	_	7.5	17	ns
Turn OFF Time (S, \overline{OE} to Output)	tOFF	R _L =50 Ω, C _L =5 pF	$\textbf{3.3}\pm\textbf{0.3}$		3.3	10	ns
Break Before Make	TBBM	RL=50 Ω, CL=5 pF	3.3 ± 0.3	2		7.0	ns
Output skew between center port to any other port (Note)	tsk(O)	C _L =5 pF	$\textbf{3.3}\pm\textbf{0.3}$	_	0.1	_	ns
Skew of Opposite Transitions of the same output (tp_{HL}- tp_{LH}) (Note)	t _{SK(P)}	C _L =5 pF	$\textbf{3.3}\pm\textbf{0.3}$		0.1		ns
Off Isolation (Non-Adjacent)	OIRR	R _T =50 Ω, f=240 MHz	3.3 ± 0.3		-36		dB
Crosstalk(Non-Adjacent)	XTalk	R _T =50 Ω, f=240 MHz	3.3 ± 0.3		-36		dB
-3dB Bandwidth	BW	R _T =50 Ω,C _L =0 pF	$\textbf{3.3}\pm\textbf{0.3}$	_	720	_	MHz

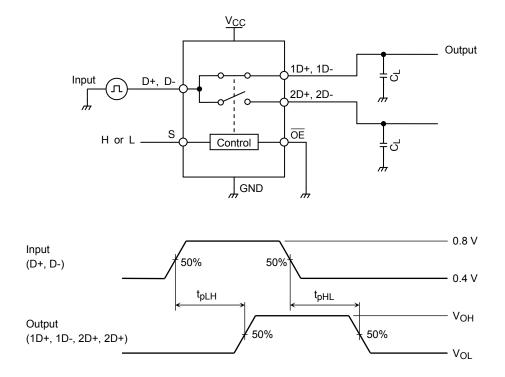
Note: This parameter is guaranteed by design.

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition		V _{CC} (V)	Тур.	Unit
Control pin input capaci tance (OE , S)	C _{IN}	$V_{IN} = 0 V $ (N	Note)	3.3	4	pF
Switch terminal Off capacitance $(D+, D-)$	C _{I/O}	$V_{IS} = 0 V, \overline{OE} = V_{CC}$ (N	Note)	3.3	4	pF
Switch terminal Off capacitance (1D+, 1D-, 2D+, 2D-)	C _{I/O}	$V_{IS} = 0 V, \overline{OE} = V_{CC}$ (N	Note)	3.3	3	pF
Switch terminal On capacitance	C _{I/O}	$V_{IS} = 0 V, \overline{OE} = GND$ (N	Note)	3.3	7	pF

Note: This parameter is guaranteed by design.

AC Test Circuit Load/Waveform





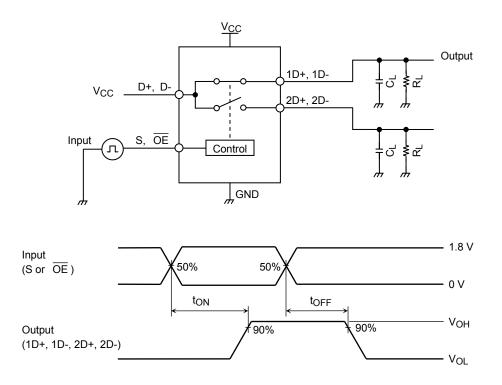


Figure 2 : Turn ON/Turn OFF (ton, toff)

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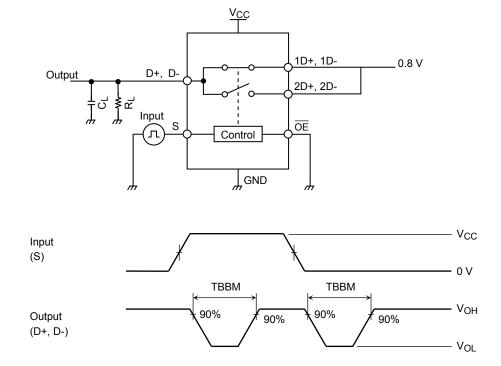
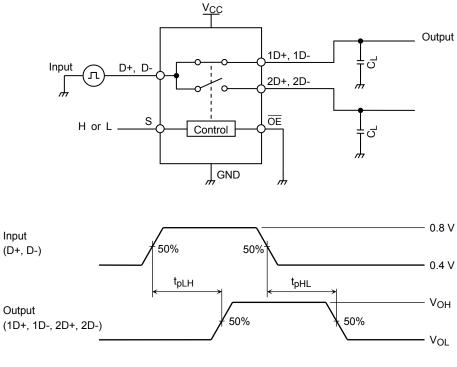
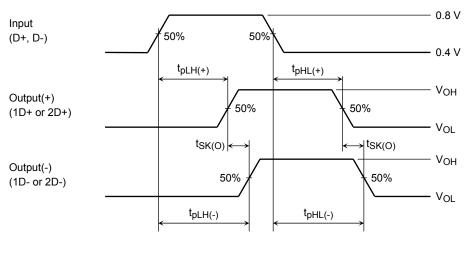


Figure 3 : Break Before Make (TBBM)

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PULSE SKEW t_{SK(P) =} |t_{pLH} - t_{pHL}|



 $\label{eq:output} \textbf{OUTPUT SKEW} \quad t_{SK(O)} = |t_{pLH(+)} - t_{pLH(-)}| \ \textbf{or} \ |t_{pHL(+)} - t_{pHL(-)}|$

Figure 4 : Skew of Opposite Transitions of the same output, Output skew

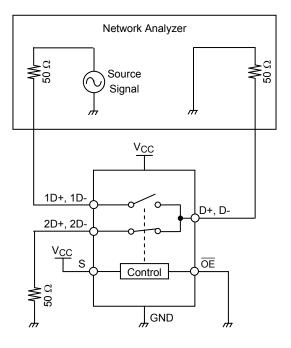


Figure 5 : Channel OFF Isolation

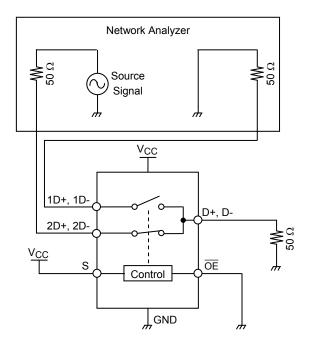


Figure 6 : Crosstalk

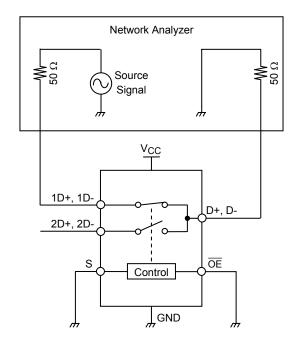


Figure 7 : -3dB Bandwidth

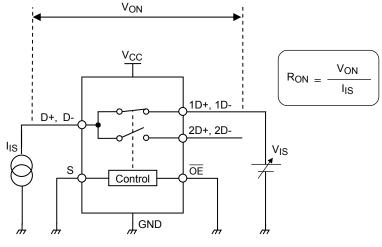


Figure 8 : ON Resistance

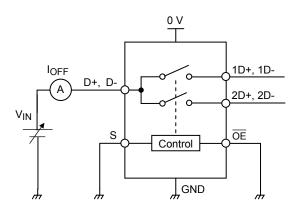
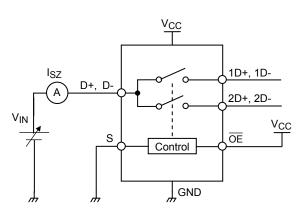


Figure 9 : Power off Leakage Current



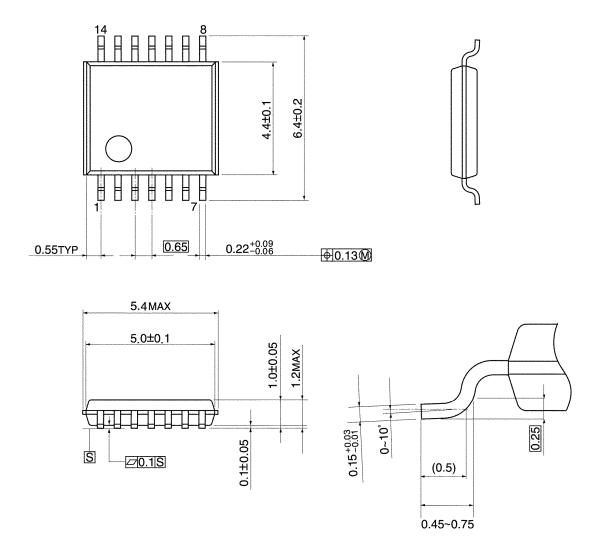




Package Dimension

TSSOP14-P-0044-0.65A

Unit: mm



Weight: 0.06 g (Typ.)

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